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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,327	02/13/2004	Dennis Wendell	SUN040316	5224

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EXAMINER	
LAM, DAVID	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/779,327	WENDELL, DENNIS	
	Examiner	Art Unit	
	David Lam	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4-10,14-20 and 24-30* is/are allowed.

6)☒ Claim(s) *1-3,11-13 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to amendment file on 9/19/05.

- Claims 1-30 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 21-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirose et al. (5,544,105).

Regarding to claims 1-3, Hirose et al. discloses a memory system comprising: a memory cell (MC), first and second bit lines (BIT, /BIT) operable to the memory cell; a write line (WL) operable connected to the memory cell and an equilibration circuit (LB) connected to the first and second bit lines, wherein the equilibration circuit is operable to maintain a predetermined equilibrium condition between the first and second bit lines and wherein the equilibration circuit is controlled by a reference voltage (WEp) and operable to generate an impedance load in the first and second bit lines at a level that allows generation of differential signals in the bit lines; wherein the equilibration circuit comprises first and second pMOS (P41, P42) devices in series with the first and second bit lines, respectively, and a third pMOS device (PE41) connected

between the first and second bit lines and wherein the gate of the first, second and third pMOS devices are connected to the reference voltage. *See Figs. 25, 27; Cols. 25-27, 29-30.*

As of claims 21-23, Hirose et al. discloses a digital processing system comprising: a data path module (602); a control module (600); an input/output module (I/O blocks); a memory cell (MC), first and second bit lines (BIT, /BIT) operable to the memory cell; a write line (WL) operable connected to the memory cell and an equilibration circuit (LB) connected to the first and second bit lines, wherein the equilibration circuit is operable to maintain a predetermined equilibrium condition between the first and second bit lines and wherein the equilibration circuit is controlled by a reference voltage (WEp) and operable to generate an impedance load in the first and second bit lines at a level that allows generation of differential signals in the bit lines; wherein the equilibration circuit comprises first and second pMOS (P41, P42) devices in series with the first and second bit lines, respectively, and a third pMOS device (PE41) connected between the first and second bit lines and wherein the gate of the first, second and third pMOS devices are connected to the reference voltage. *See Figs. 25, 27, 45-46, 57; Cols. 25-27, 29-30.*

With regard to claims 11-13, they encompass the same scope of invention as to that of claims 1-3, 21-23 except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Response to Arguments

Applicant's arguments filed on 9/19/05 have been fully considered but they are not persuasive.

With respect to Applicant's arguments on pages 10-11 of the remarks, "the LB circuit is not an equilibration circuit." The Examiner disagrees with this statement, although Hirose et al. (5,544,105) not explicitly call LB an equilibration circuit. However, the LB includes pMOS transistors 41, 42 which conduct in response equalize/pre-charge signal for equalize/pre-charge bit lines potential, it would have been known to a person have ordinary skill in the art the LB is an equilibration circuit. Thus, the rejection of claims 1-3, 11-13, 21-23 set forth above is proper.

Allowable Subject Matter

3. The following is an examiner's statement of reasons for allowance: Claims 4-10, 14-20, 24-30 are allowable over the prior art of record because none of the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach: method and apparatus of a memory system comprising an equilibration circuit, among others as claimed in independent claims 4, 14, 24, comprises first and second Pmos in series with first and second bit lines, respectively, and a third pMOS connected between the first and second bit lines and having gate connected to the gate of the first and second pMOS to a reference voltage, wherein the pMOS operable as resistors in a linear region of MOSFET device.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Lam whose telephone number is 571-272-1782. The examiner can normally be reached on 6:00 – 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852852. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Lam

November 25, 2005

DAVID LAM
PRIMARY EXAMINER